AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method of routing a design in a programmable logic device (PLD) to increase the effectiveness of applying a multi-frame write (MFW) technique, the method comprising:

analyzing logic placement in the design;

generating a list of placement patterns as a result of analyzing the logic placement, the list of placement patterns including a list of nets associated with each placement pattern;

wherein each net includes a source and one or more loads, and each net associated with a placement pattern has placement of the source relative to placement of the loads identical to each other net associated with the placement pattern;

sorting the list of placement patterns in an order determined by a number of nets associated with each placement pattern; [[and]]

routing the nets associated with each placement pattern, in order from a placement pattern having a largest number of nets to a placement pattern having a smaller number of nets; and

wherein the routing includes, in response to a placement pattern having more than two associated nets, determining whether more than two nets associated with the placement pattern are routable with one selected routing template, wherein a routing template specifies relative routing resources that represent a pattern of a possible route for all the nets associated with the placement pattern, and in response to determining that more than two nets associated with the routing pattern are routable with the one selected routing pattern, routing the more than two nets consistent with the one selected routing template.

2. (Original) The method of Claim 1, wherein the smaller number of nets is a predetermined threshold number.

3. (Original) The method of Claim 2, wherein the predetermined threshold number is four.

4. (Original) The method of Claim 1, wherein routing the nets associated with each placement pattern results in a fully routed design, the method further comprising:

generating a configuration bitstream for the fully routed design; and

compressing the configuration bitstream using an MFW technique.

5. (Original) The method of Claim 1, wherein routing the nets associated with each placement pattern does not result in a fully routed design, the method further comprising:

routing the nets associated with the placement patterns having a number of nets less than the smaller number of nets to produce a fully routed design.

6. (Original) The method of Claim 5, further comprising:

generating a configuration bitstream for the fully routed design; and

compressing the configuration bitstream using an MFW technique.

7. (Currently Amended) A method of routing a design in a programmable logic device (PLD) to increase the effectiveness of applying a multi-frame write (MFW) technique, the method comprising:

analyzing logic placement in the design;

generating a list of placement patterns as a result of analyzing the logic placement, the list of placement patterns including a list of nets associated with each placement pattern;

sorting the list of placement patterns in an order determined by a number of nets associated with each placement pattern;

routing the nets associated with each placement pattern, in order from a placement pattern having a largest number of nets to a placement pattern having a smaller number of nets; and

~~The method of Claim 1,~~ wherein routing the nets associated with each placement pattern comprises, for each placement pattern:

selecting a plurality of sample nets from the list of nets associated with the placement pattern;

generating a plurality of routing templates for each sample net and adding the routing templates to a cache of routing templates;

selecting from the cache of routing templates a best template for unrouted nets associated with the placement pattern; and

routing each unrouted net that can be routed using the best template.

8. (Original) The method of Claim 7, further comprising:

sorting, within the list of placement patterns, the list of nets associated with each placement pattern based on physical locations of the nets within the PLD,

and wherein selecting a plurality of sample nets from the list of nets associated with the placement pattern comprises selecting from the list of nets associated with the placement pattern a plurality of nets having origins located in different physical areas of the PLD.

9. (Original) The method of Claim 7, wherein selecting from the cache of routing templates a best template for unrouted nets associated with the placement pattern comprises:

calculating, for each routing template in the cache of routing templates, a number of nets associated with the placement pattern that are not yet routed but can be routed using the routing template; and

selecting as the best template a routing template that can be applied to a largest number of nets.

10. (Original) The method of Claim 7, wherein selecting from the cache of routing templates a best template for unrouted nets associated with the placement pattern comprises:

calculating, for each routing template in the cache of routing templates, a number of nets associated with the placement pattern that are not yet routed but can be routed using the routing template;

determining a set of routing templates that can be used to route at least a given percentage of remaining unrouted nets; and

selecting from the set of routing templates as the best template a routing template that uses a largest number of previously unused routing resources in the PLD.

11. (Original) The method of Claim 1, wherein the PLD is a field programmable gate array (FPGA).

12. (Currently Amended) A computer-readable storage medium comprising computer-executable code for routing a design in a programmable logic device (PLD) to increase the effectiveness of applying a multi-frame write (MFW) technique, the medium comprising:

code for analyzing logic placement in the design;

code for generating a list of placement patterns as a result of analyzing the logic placement, the list of placement patterns including a list of nets associated with each placement pattern;

code for sorting the list of placement patterns in an order determined by a number of nets associated with each placement pattern; [[and]]

code for routing the nets associated with each placement pattern, in order from a placement pattern having a largest number of nets to a placement pattern having a smaller number of nets; and

wherein the code for routing the nets associated with each placement pattern comprises, for each placement pattern:

code for selecting a plurality of sample nets from the list of nets associated with the placement pattern;

code for generating a plurality of routing templates for each sample net and adding the routing templates to a cache of routing templates;

code for selecting from the cache of routing templates a best template for unrouted nets associated with the placement pattern; and

code for routing each unrouted net that can be routed using the best template.

13. (Original) The medium of Claim 12, wherein the smaller number of nets is a predetermined threshold number.

14. (Original) The medium of Claim 13, wherein the predetermined threshold number is four.

15. (Original) The medium of Claim 12, wherein the code for routing the nets associated with each placement pattern provides a fully routed design, the medium further comprising:

code for generating a configuration bitstream for the fully routed design; and

code for compressing the configuration bitstream using an MFW technique.

16. (Original) The medium of Claim 12, wherein the code for routing the nets associated with each placement pattern does not provide a fully routed design, the medium further comprising:

code for routing the nets associated with the placement patterns having a number of nets less than the smaller number of nets to produce a fully routed design.

17. (Original) The medium of Claim 16, further comprising:

code for generating a configuration bitstream for the fully routed design; and

code for compressing the configuration bitstream using an MFW technique.

Claim 18. (Cancelled)

19. (Currently Amended) The medium of Claim 12 [[18]], further comprising:

code for sorting, within the list of placement patterns, the list of nets associated with each placement pattern based on physical locations of the nets within the PLD,

and wherein the code for selecting a plurality of sample nets from the list of nets associated with the placement pattern comprises code for selecting from the list of nets associated with the placement pattern a plurality of nets having origins located in different physical areas of the PLD.

20. (Currently Amended) The medium of Claim 12 [[18]], wherein the code for selecting from the cache of routing templates a best template for unrouted nets associated with the placement pattern comprises:

code for calculating, for each routing template in the cache of routing templates, a number of nets associated with the placement pattern that are not yet routed but can be routed using the routing template; and

code for selecting as the best template a routing template that can be applied to a largest number of nets.

21. (Currently Amended) The medium of Claim 12 [[18]], wherein the code for selecting from the cache of routing templates a best template for unrouted nets associated with the placement pattern comprises:

code for calculating, for each routing template in the cache of routing templates, a number of nets associated with the placement pattern that are not yet routed but can be routed using the routing template;

code for determining a set of routing templates that can be used to route at least a given percentage of remaining unrouted nets; and

code for selecting from the set of routing templates as the best template a routing template that uses a largest number of previously unused routing resources in the PLD.

22. (Original) The medium of Claim 12, wherein the PLD is a field programmable gate array (FPGA).

23. (Currently Amended) A computer system for routing a design in a programmable logic device (PLD) to increase the effectiveness of applying a multi-frame write (MFW) technique, the system comprising:

a logic analyzing module for analyzing logic placement in the design;

a list generation module for generating a list of placement patterns as a result of analyzing the logic placement, the list of placement patterns including a list of nets associated with each placement pattern;

a first sorting module for sorting the list of placement patterns in an order determined by a number of nets associated with each placement pattern; and

a first routing module for routing the nets associated with each placement pattern, in order from a placement pattern having a largest number of nets to a placement pattern having a smaller number of nets; and

wherein the first routing module comprises, for each placement pattern:

a sampling module for selecting a plurality of sample nets from the list of nets associated with the placement pattern;

a template generating module for generating a plurality of routing templates for each sample net and adding the routing templates to a cache of routing templates;

a template selection module for selecting from the cache of routing templates a best template for unrouted nets associated with the placement pattern; and

a net routing module for routing each unrouted net that can be routed using the best template.

24. (Original) The computer system of Claim 23, wherein the smaller number of nets is a predetermined threshold number.

25. (Original) The computer system of Claim 24, wherein the predetermined threshold number is four.

26. (Original) The computer system of Claim 23, wherein the first routing module provides a fully routed design, the computer system further comprising:

a bitstream generation module for generating a configuration bitstream for the fully routed design; and

a bitstream compression module for compressing the configuration bitstream using an MFW technique.

27. (Original) The computer system of Claim 23, wherein the first routing module does not provide a fully routed design, the computer system further comprising:

a second routing module for routing the nets associated with the placement patterns having a number of nets less than the smaller number of nets to produce a fully routed design.

28. (Original) The computer system of Claim 27, further comprising:

a bitstream generation module for generating a configuration bitstream for the fully routed design; and

a bitstream compression module for compressing the configuration bitstream using an MFW technique.

Claim 29. (Cancelled)

30. (Currently Amended) The computer system of Claim 23 [[29]], further comprising:

a second sorting module for sorting, within the list of placement patterns, the list of nets associated with each placement pattern based on physical locations of the nets within the PLD,

and wherein the sampling module comprises code for selecting from the list of nets associated with the placement pattern a plurality of nets having origins located in different physical areas of the PLD.

31. (Currently Amended) The computer system of Claim 23 [[29]], wherein the template selection module comprises:

a calculation module for calculating, for each routing template in the cache of routing templates, a number of nets associated with the placement pattern that are not yet routed but can be routed using the routing template; and

a best template selection module for selecting as the best template a routing template that can be applied to a largest number of nets.

32. (Currently Amended) The computer system of Claim 23 [[29]], wherein the code for selecting from the cache of routing templates a best template for unrouted nets associated with the placement pattern comprises:

a calculation module for calculating, for each routing template in the cache of routing templates, a number of nets associated with the placement pattern that are not yet routed but can be routed using the routing template;

a template set selection module for determining a set of routing templates that can be used to route at least a given percentage of remaining unrouted nets; and

a best template selection module for selecting from the set of routing templates as the best template a routing template that uses a largest number of previously unused routing resources in the PLD.

33. (Original) The computer system of Claim 23, wherein the PLD is a field programmable gate array (FPGA).